REMARKS

Claims 1-39, and 47-62 are presently pending in the application. Applicant has amended Claim 28 to more clearly describe that which was previously claimed. Applicant acknowledges the withdrawal of the restriction requirement. Applicant has added new claims 57-62, which are supported in the specification and are not new matter.

Claims 1-6, 34-39, 47-50, and 52-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai et al. (hereinafter Lai), in view of U.S. Pat. No. 5,870,294 (hereinafter Cyr). Claims 7-11 and 13-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai in view of Cyr, and further in view of U.S. Pat. No. 5,923,152 (hereinafter Guerrera). Claims 12, 19-33, and 51 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai in view of Cyr, and further in view of Pinheiro et al. (hereinafter Pinheiro).

Applicant has organized this response with reference to each independent claim.

A. Claim 1 and related dependent Claims 2-7, and 56 are allowable because the asserted combination does not describe each and every limitation of the respective claims.

Claim 1 describes "the first and second boost converters are configured to receive an input voltage and supply a boost voltage." Applicant traverses the assertion that "Lai describes the invention substantially as claimed" except for "a power factor correction configured to control boost converters with pulse modulation," *see* Office Action, Item 2, pgs. 2-3, because Lai describes neither a boost converter nor a boost sub-circuit. Instead, Lai describes a multileveled voltage source converter to synthesize a staircase voltage output that approximates a sinusoid, which is clearly not a boost voltage as described in Claim 1. *See* Lai's abstract; *see also* Lai's Fig. 2.

Specifically, Lai describes switches Sa4 through Sa'4a and diodes Da4 through Da'4 forming a "positive phase-leg a" of the multi-leveled voltage source converter, *see* Lai's Fig. 1, not a boost sub-circuit or a first and second boost converter, as described in Claim 1. *See* Section

II, A. Basic Principle (bottom of Col. 2, page 1.) In Lai, the input DC bus voltage, Vdc, is placed across series capacitors C1, C2, C3 and C4, where there is approximately ¼ of Vdc across each of the capacitors (C1, C2, C3 and C4). *See id.* Lai describes switching switches Sa4 through Sa'4 to connect a fractional portion of the input voltage, Vdc, to the output at Node "a" (Vcab) to form a staircase output voltage Va0. *See* Lai's Fig. 2. Moreover, Lai describes the switches function as: "1) For voltage level Va0=Vdc, turn on all upper switches Sa1 through Sa4. ... 3) For voltage level Va0=Vdc/2, turn on two upper switches Sa3 and Sa4 and two lower switches Sa'1 and Sa'2....5) For voltage level Va0=0, turn on all lower half switches Sa'1 through Sa'2," where Va0 is the output at Node "a" (Vcab) during operation of the "positive phase-leg a." *See* Lai, Col. 2, bottom, pg. 1 – Col. 1, middle, pg. 2.

Referencing Fig. 1 of Lai, to provide an output Va0=Vdc, Lai describes turning on switches Sa1, Sa2, Sa3, and Sa4 to connect the output Node "a" (Vcab) to input Node "V5", which has voltage Vdc relative to Node "V1." To provide an output Va0=0, Lai describes turning on switches Sa'1, Sa'2, Sa'3, and Sa'4 to connect the output Node "a" (Vcab) to Node "V1." *See id.* As further described in Lai, when Sa'1 – Sa'4 are turned on, Da'1 blocks the voltage 3Vdc/4 from Node V4 while Da2 and Da'2 block the voltage at Node V3. *See* Lai, Col. 2, page 2 (at Section II.B "Features").

Finally, to provide an output Va0-Vac/2, Lai describes turning on switches Sa3 and Sa4 to connect a first current path between Node V3 and Node "a" (Vcab) while turning on switches Sa'1 and Sa'2 to connect a second current path between Node V3 and Node "a" (Vcab). *See id.* The first current path allows current from Node V3 to pass through the connecting diodes and Sa3 and Sa4 to Node "a" (Vcab). The second current path allows current from Node "a" (Vcab) to pass through the connecting diodes and Sa'1 and Sa'2 to V3. Operating together, the first and second current paths of Lai connect Node V3 to Node "a" (Vcab).

Thus, Lai clearly describes switches Sa4 - Sa'4 and Da4 - Da'4 selectively connecting the fractions of the input voltage, Vdc, that are across C1, C2, C3, and C4 to Lai's output at Node "a"

(Vcab). As confirmed in Fig. 2 and Table I, the output Va0 has a maximum magnitude that is **not greater in magnitude than a peak magnitude of the input voltage**, Vdc. Fig. 2. In addition, Table I of Lai explicitly shows the output at Node "2" (Vcab) is a fraction of the input voltage, Vdc, depending upon the switches position. As a result, Lai does not describe "a boost voltage that is greater in magnitude than a peak magnitude of the input voltage," as described in Claim 1.

Applicant also traverses the rejection's assertion that Lai's Sa1, Da1, C1 / Sa2, Da2, C2 form a "first boost converter", Lai's Sa3, Da3, C3 / Sa4, Da4, C4 form a "second boost converter", or that the respective groupings {Sa1, Da1, C1}, {Sa2, Da2, C2}, {Sa3, Da3, C3}, or {Sa4, Da4, C4} form respective first, second, third and forth boost sub-circuits. As previously discussed, the input voltage, Vdc, is fractionally distributed across capacitors C1, C2, C3, and C4. Lai's Sa1 - Sa4 and Da1 - Da4 couple the output Node "a" (Vcab) to the fractional voltages stored on capacitors C1 through C4. *See* Lai, Col. 2, bottom; *see also* Fig. 3(a) (showing C1, C2, C3 and C4 related to V1, V2, V3, V4, and V5, respectively). Lai does not describe any combination of switches Sa4-Sa'4 that result in Lai's multileveled voltage source converter supplying a boost voltage [at the output Node "a"] that is greater in magnitude than a peak magnitude of the input voltage [Vdc at Node V5]. Instead, Lai describes generating voltages at the output Node "a" that have a magnitude that is a fraction of the input voltage, Vdc. *See* Lai's Fig. 2. Thus, Lai does not describe even a first boost converter. As a result, the asserted component combinations {Sa1, Da1, C1}, {Sa2, Da2, C2}, {Sa3, Da3, C3}, and {Sa4, Da4, C4} do not describe a respective first, second, third, and forth boost sub-circuits, as Claim 1 describes, because the sub-groups described in Lai provide no boost to the input voltage. Moreover, Cyr does not describe, as Claim 1 describes, "a second boost converter coupled in series with the first boost converter" or a boost converter including "a first boost sub-circuit and a second boost sub circuit." As a result, the asserted combination does not describe, as Claim 1 describes, "a first boost sub-circuit coupled with a second boost sub-circuit", "a third boost sub-

circuit coupled with a fourth boost sub-circuit", or "a second boost converter coupled in series with the first boost converter."

Moreover, even assuming for the sake of argument that Lai is modified by Cyr as asserted in the Office Action mailed December 4, 2006, to include pulse width modulation of switches Sa4-Sa'4, the asserted modified circuit would not provide a boosted output. To the contrary, pulse width modulation of Lai's switches Sa4-Sa'4 would only change the timing (or width) of the steps in the multilevel sinusoid approximation because the switches merely operate to connect the output at Node "a" to a fractional portion of the input voltage, Vdc, across C1, C2, C3 and C4. Thus, even with the asserted modification the peak magnitude of the output voltage at Node "a" would still never be more than Vdc. Accordingly, the asserted combination fails to supply a boost voltage that is greater in magnitude than a peak magnitude of the input voltage as described in Claim 1. Therefore, the rejection should be withdrawn because the asserted combination fails to describe each and every element of Claim 1.

In conclusion, for at least these reasons, Applicant request that the rejection of Claim 1 be withdrawn. In addition, dependent Claims 2-7 and 56 are allowable at least for the reason that independent Claim 1 is in allowable form.

B. Claim 8 and related dependent Claims 9-18 are allowable because the asserted combination does not describe each and every limitation of the claims at issue.

Claim 8 describes "a power factor correction controller ... configured to provide a DC boost voltage from the input voltage." Claim 8 also describes a "power factor correction controller configured to direct the at least four boost switches independently with interleave to provide a DC boost voltage." Applicant respectfully traverses the assertion on pg. 3 of the Office Action mailed December 4, 2006, that "Lai et al as modified by Cyr describes the invention substantially as claimed" except for "boost switches that are independently switchable," because the asserted combination does not describe "an input stage converter that

includes at least four boost switches coupled in series," or "a power factor correction controller coupled with the at least four boost switches" or "a power factor correction controller [] configured ... to direct the at least four boost switches as a function of the DC boost voltage."

First, Lai in view of Cyr does not describe a "DC boost voltage." Instead, as previously discussed, Lai describes a multilevel voltage source converter that produces a staircase output having m-levels to approximate a sinusoid, *see* Lai's Fig. 2. Clearly, Lai's staircase output that approximates a sinusoid, which is not a DC boost voltage, as described in Claim 8. Second, neither Lai, Cyr, nor Guerrera describe four boost switches. Third, even assuming the asserted combination, where Lai is modified to include both pulse width modulation and independently controlled switches, the asserted combination would only change the timing (or width) of the steps in the multilevel sinusoid approximation at Lai's output, Node "a" (Vcab), because Lai's switches merely connect Lai's output at Node "a" to a fractional portion of the input voltage, Vdc. As a result, the circuit of Lai with the asserted modification of Cyr and Guerrera would still only produce the approximated sinusoid as shown in Fig. 2. In other words, the asserted combination would not provide a boost voltage or a DC voltage output.

Furthermore, the proposed modification of Lai to include "independently control switches" is improper because Lai teaches directly against the modification. A rejection is improper when the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." *See* MPEP § 2143.01 (*citing In re Ratti*, 270 F.2d at 813, 123 USPQ at 352). Lai directly recites that "the complimentary switch pair is defined such that turning on one of the pair switches will exclude the other from being turned on." *See* Lai, Col. 1, page 2. As a result, Lai explicitly describes the switches' position must be "dependent." The asserted modification to provide "independently controlled switches" is improper because the modification would "change the basic principle under which" Lai's "construction was designed to operate." *See* MPEP § 2143.01.

Moreover, modifying Lai to provide a DC boost voltage would also require a fundamental change in the basic principle of operation and construction of Lai, because Lai produces an approximated sinusoidal output that is not boosted, as previously discussed.

As a result, for at least these reasons, the rejection of Claim 8 does not establish *prima facie* obviousness because the asserted combination fails to describe each and every limitation, and is otherwise improper because the asserted modification would change the fundamental operation of Lai. Therefore, Claim 8 is in allowable form. In addition, the rejection of the dependent Claims 9-18 should be withdrawn because the independent Claim 8 is in allowable form. For at least these reasons, Claims 9-18 are also in form for allowance.

C. Claim 19 and related dependent Claims 20-27 are allowable because the asserted combination does not describe each and every limitation of the claims at issue.

Claim 19 describes "an input stage power converter that includes ... the first boost converter coupled in series with a second boost converter ... to supply a DC boost voltage." Applicant traverses the rejection's assertion that "Lai as modified by Cyr describes the invention substantially claimed" except for "a converter configured to balance the boost voltage," *see* Office Action, Item 5, pg. 4, because the asserted combination would not provide a boosted output or a dc boost output.

Specifically, Lai describes a staircase output without boost that approximates a sinusoid. *See* Lai's Fig. 2. The asserted modification of Lai with Cyr would also not provide a boost voltage because Lai's switches Sa4-Sa'4 and Da4-Da'4 merely couple the output Node "a" (Vcab) to a fraction of the input voltage, Vdc. *See* Lai's Table I. Furthermore, modifying the timing of Lai's switches only moves the edge of the step (the width) without providing a boost or a DC boost voltage at the output. Thus, Lai clearly does not describe "**to supply a DC boost voltage**," as described in Claim 19. Accordingly, because Lai as modified by Cyr does not describe "the invention as substantially claimed," the boost voltage, "the proposed combination does not show

each and every limitation of Claim 19. Moreover, the asserted combination of Lai with Cyr is improper because the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in" Lai "as well as a change in the basic principle under which" Lai's "construction was designed to operate" because Lai produces a multilevel staircase output to approximate a sinusoid, not a DC output nor a boost output as described in Claim 19. *See,* MPEP § 2143.01 (*citing In re Ratti*, 270 F.2d at 813, 123 USPQ at 352).

In addition, even if the assertion on pg. 4 of the Office Action mailed December 4, 2007, that Pinheiro describes "the use of boost power factor correction configured to balance the boost voltage" is correct, the proposed modification would not result in the invention described in Claim 19 because Lai's circuit as modified does not provide a boost voltage or multiple outputs to be balanced. To the contrary, Lai has only a single output, Node "a" (Vcab), which never exceeds the input voltage, Vdc. Thus, Lai does not describe multiple outputs for Pinheiro to modify which has apparently been asserted. Accordingly, the proposed modification is both inoperable and does not yield a DC boost voltage. As a result, the proposed combination does not establish *prima facie* obviousness.

Finally, Applicant traverses the rejections based merely upon Pinheiro's general statement that "[b]esides the features of the three-level boost converter already known" because a general assertion that is not "at all specific as to the particular form of the claimed invention and how to achieve it" is insufficient to establish obviousness. *See, ex parte* Obukowcz.

For at least these reasons, the rejection of Claim 19 should be withdrawn. As a result, Claim 19 is in condition for allowance. Also, the rejection of dependent Claims 20-27 should be withdrawn at least for the reasons that independent Claim 19 is in allowable form.

D. Independent Claim 28 and dependent Claims 29-33 are allowable because the asserted combination does not describe each and every limitation of the respective claims.

Claim 28 describes a "first and second pair of boosts switches with interleave to provide a portion of a DC boost voltage." Applicant traverses the rejection of the independent Claim 28 based upon the assertion that "Lai as modified by Cyr describes the invention substantially claimed "except for a converter configured to balance the boost voltage," and further asserting Pinheiro shows "the use of boost power factor correction configuration to balance the boost voltage is well known in the art," *see,* Office Action, Item 5, pg. 4, because the asserted combination does not describe "the first and the second pair of boost switches [controlled] with interleave to provide a portion of DC boost voltage" or "the output stage power converters ... configured to substantially balance ...the DC boost voltage," as described in Claim 28.

To the contrary, Lai describes producing a multilevel staircase output that approximates a sinusoidal output at Node "a" without any boost, *see* Lai's Fig. 2, which is clearly not a boost supply nor a portion of a DC boost voltage as described in Claim 28. Moreover, as discussed previously, modifying Lai with Cyr would not result in a boost voltage because Lai's switches are only configured to couple a fractional portion of the input, Vdc, to the output Node "a" (Vcab). Finally, even assuming the further asserted modification of "a boost power factor correction to balance the boost voltage," *see* Office Action pg. 4, there would still be no DC boost output because Lai describes a single output Node "a" (Vcab). Thus, the asserted modified Lai does not have an output to balance, and clearly does not provide a boosted output or a DC output.

Moreover, neither Lai nor Cyr describe a "first and the second pair of boost switches are coupled in series," as described by Claim 28. Also, Pinheiro does not describe "the first and the second pair of boost switches are coupled in series" because Pinheiro only describes two switches S1 and S2. *See* Col. 2, page 1 – Col. 1, page 2. As a result, the asserted combination

of Lai, Cyr and Pinheiro does not show a "first and second pair of boost switches ... coupled in series," as claim 28 describes.

Therefore, the asserted combination of references does not teach or suggest each and every limitation of Claim 28. Thus, Claim 28 is in condition for allowance. Rejection of dependent Claims 29-33 should also be withdrawn at least because independent Claim 28 is in allowable form.

E. Claim 34 and related dependent Claims 35-39 are allowable because the asserted combination does not describe a DC boost voltage.

Claim 34 describes "the first and second boost switches and the first and second boost sub-switches are switchable with pulse width modulation to develop at least a portion of a DC boost voltage on the boost capacitor" and the "DC boost voltage is greater in magnitude than a peak magnitude of the AC input voltage." Applicant traverses the asserted combination that states "Lai describes the invention substantially as claimed" except for "a power factor correction configured to control boost converters with pulse modulation," where Cyr describes a "power factor corrector with boost topology driven by conditional PWM drive signals," *see* Office Action, pgs. 2-3, because Lai describes a multileveled voltage source converter to synthesize a staircase voltage output that approximates a sinusoid where the peak magnitude of the output is not greater than the peak magnitude of the input voltage, Vdc. Thus, the asserted combination clearly does not describe either developing a DC boost voltage or a DC boost voltage greater in magnitude than a peak amplitude of the AC input, as described in Claim 34.

First, Lai does not produce a DC output, as described in Claim 34, because Lai produces an approximated sinusoidal staircase voltage. *See* Lai's Fig. 2. Moreover, Lai does not produce a boost voltage, as also described in Claim 34, because the switches Sa4-Sa'4 and Da4-Da'4 are used to connect the output Node "a" (Vcab) to a fractional portion of the input voltage, Vdc. *See* Lai's Table I and Fig. 2. Thus, even if, for the sake of argument, the asserted modification was

made to Lai, the resulting combination would only modify the placement of the stair step edges (width), but not the peak magnitude of the output, because Lai does not describe a boost converter or a boost sub-circuit, as described in Claim 34. Thus, the asserted combination does not describe each and every limitation of Claim 34.

Finally, applicant traverses the asserted combination as improper because modifying Lai from producing a non-boosted staircase approximated sinusoid to produce a DC voltage or a boost voltage would "require a substantial reconstruction and redesign of the elements shown in" Lai "as well as a change in the basic principle under which" Lai's "construction was designed to operate." *See* MPEP § 2143.01 (*citing In re Ratti*, 270 F.2d at 813, 123 USPQ at 352).

Thus, for at least these reasons, the rejection of independent Claim 34 does not establish *prima facie* obviousness, and Claim 34 is allowable. In addition, Applicant respectfully submits that dependent Claims 35-39 are allowable at least because independent Claim 34 is in condition for allowance.

F. Claim 47 and related dependent Claims 48-55 are allowable because the asserted combination does not describe each and every limitation of the claim at issue.

Claim 47 describes "interleave switching at least **four boost switches** that are coupled in series across the power source to convert the input voltage to a first DC voltage." Applicant traverses the rejection that Lai describes Claim 47 except for "a power factor correction controller configured to control converters with pulse modulation," *see*, Office Action, pgs. 2-3, because neither Lai nor Cyr describe "four boost switches that are coupled in series to convert the input voltage to a first DC voltage."

First, Lai does not describe any boost switches, as described in Claim 47, because the magnitude of Lai's output is no greater than the input voltage, Vdc. Second, Lai describes a multilevel staircase output that approximates a sinusoid, which is clearly not a DC voltage as described in Claim 47. Moreover, the proposed modification of further including "a power

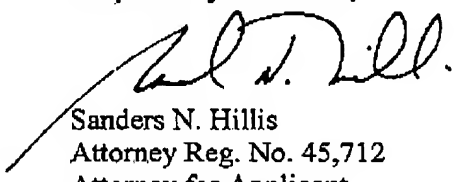
factor correction controller configured to control converters with pulse modulation" would not produce a boost voltage because Lai's switches connect a fractional portion of Lai's Vdc to Lai's output, Node "a" (Vcab). Finally, neither Lai nor Cyr describe "interleave switching four boost switches," as described in Claim 47 because, as previously discussed, neither Cyr nor Lai describe interleave switching.

As a result, the rejection of Claim 47 does not establish *prima facie* obviousness and should be withdrawn. For at least these reasons, Claim 47 is allowable. Finally, dependent Claims 48-55 are allowable at least because independent Claim 47 is in condition for allowance.

Conclusion

The application is now in condition for allowance, which Applicant earnestly requests. Should the Examiner deem a telephone conference to be beneficial in expediting examination and/or allowance of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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